

CLAIMS

What is claimed is:

CLAIM 1

- 1 A method for fabricating complementary vertical bipolar junction transistors comprising the
- 2 steps of:
- 3 providing a sapphire substrate;
- 4 forming a layer of silicon on said sapphire substrate;
- 5 recrystalizing said silicon layer;
- 6 forming a P+ region in said silicon layer to become a collector for a PNP transistor;
- 7 forming N+ region in said silicon layer to become a subcollector for an NPN transistor;
- 8 forming an N silicon layer over said P+ and N+ regions to become an intrinsic base
- 9 region for said PNP transistor and to become a collector region for said NPN transistor;
- 10 forming islands of what is to become said PNP transistor and of what is to become said
- 11 NPN transistor by removing any silicon therebetween to said sapphire substrate;
- 12 forming a P intrinsic base region in said N collector region for said NPN transistor;
- 13 forming P+ extrinsic base regions in said P intrinsic base region for said NPN transistor;
- 14 forming a P+ emitter region in said N base region for said PNP transistor;
- 15 forming an N+ emitter region in said P base region for said NPN transistor;
- 16 forming N+ extrinsic base regions in said N base region for said PNP transistor; and
- 17 forming individual conducting metal contacts with said emitters and extrinsic bases, said
- 18 individual conducting metal contacts being formed between oxide regions.

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CLAIM 2

1 The method according to claim 1 wherein said recrystallization is done by a double solid phase
2 epitaxy technique.

CLAIM 3

1 The method according to claim 1 wherein said silicon layer formed on said sapphire substrate is
2 approximately 0.3 micrometers thick.

CLAIM 4

1 The method according to claim 1 wherein said N, N+, P and P+ regions are created through ion
2 implantation.

CLAIM 5

1 The method according to claim 1 wherein said N-type silicon layer is approximately 2.5
2 micrometers thick.

CLAIM 6

1 The method according to claim 1 wherein arsenic ion implantation is used to produce said N-type
2 and N+-type regions.

CLAIM 7

1 The method according to claim 1 wherein boron ion implantation is used to produce said P-type

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and P+-type regions.

CLAIM 8

The method of claim 1 further including the steps of:

forming P+ collector plugs in said N base region for said PNP transistor so that said P+ collector plugs are incorporated into said P+ collector for said PNP transistor;

forming N+ collector plug regions in said N collector region for said NPN transistor so that said N+ collector plugs are incorporated into said N+ sub-collector region for said NPN transistor;

forming individual conductive metal contacts with said collector plug regions; and

forming an oxide region between said collector plug metal contacts.

CLAIM 9

The method according to claim 8 wherein said N, N+, P and P+ regions are created through ion implantation.

CLAIM 10

The method according to claim 8 wherein arsenic ion implantation is used to produce said N-type and N+-type regions.

CLAIM 11

The method according to claim 8 wherein boron ion implantation is used to produce said P-type

and P+-type regions.

CLAIM 12

A complementary vertical bipolar junction transistor apparatus comprising:

a sapphire substrate;

a PNP transistor including:

a P+ region formed of an island of recrystallized silicon disposed on said sapphire substrate, said P+ region being a collector region;

an N silicon region disposed within said P+ region, said N silicon region being an intrinsic base region;

a P+ emitter region disposed within said N base region;

N+ extrinsic base regions disposed within said N base region;

individual conducting metal contacts operably coupled to said emitter, said extrinsic base regions and disposed on sidewalls of said collector region; and

an oxide disposed between said conducting metal contacts;

a NPN transistor including:

an N+ region formed of an island of recrystallized silicon disposed on said sapphire substrate and separated from said PNP transistor, said N+ region being a subcollector region;

an N silicon region disposed within said N+ region, said N silicon region being a collector region;

a P intrinsic base region disposed within said N collector region;

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20 an N+ emitter region disposed within said P base region;
21 forming P+ extrinsic base regions in said P intrinsic base region;
22 individual conducting metal contacts operably coupled to said emitter, said
23 extrinsic base regions and disposed on sidewalls of said collector region; and
24 an oxide region disposed between said conducting metal contacts; and
25 an oxide region disposed on said sapphire substrate between said PNP and NPN
26 transistors.

CLAIM 13

1 The apparatus according to claim 12 wherein said recrystallization is done by a double solid
2 phase epitaxy technique.

CLAIM 14

1 The apparatus according to claim 12 wherein said silicon layer on said sapphire substrate is
2 approximately 0.3 micrometers thick.

CLAIM 15

1 The apparatus according to claim 12 wherein said N, N+, P and P+ regions are created through
2 ion implantation.

CLAIM 16

1 The apparatus according to claim 12 wherein said N-type silicon layer is approximately 2.5

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2 micrometers thick.

CLAIM 17

1 The apparatus according to claim 12 wherein arsenic ion implantation is used to produce said N-
2 type and N+type regions.

CLAIM 18

1 The apparatus according to claim 12 wherein boron ion implantation is used to produce said P-
2 type and P+-type regions.